

CLAIM AMENDMENT

Please **CANCEL** claims 1-7, 9-15 and 17-23.

Please **ADD** new claims 24-43, as follows.

Sub DI
1-7. (Cancelled)

8. (Previously Cancelled)

9-15. (Cancelled)

CI
16. (Previously Cancelled)

17-23. (Cancelled)

24. (New) A method for driving a liquid crystal display (LCD) having a first gate line block and a second gate line block, the method comprising the steps of:

providing a first pixel voltage to a first pixel electrode formed in the first gate line block;

providing a second pixel voltage to a second pixel electrode formed in the second gate line block;

providing a common voltage to a common electrode;

providing a first data signal to a first data line formed in the first gate line block, said first data signal influencing a first difference between the common voltage and the first pixel voltage stored in the first pixel electrode;

providing a second data signal to a second data line formed in the second gate line block,
said second data signal influencing a second difference between the common voltage and the
second pixel voltage stored in the second pixel electrode; and
controlling the first data signal and the second data signal to simultaneously increase or
decrease the first difference and the second difference.

25. (New) The method of claim 24, wherein the first pixel voltage has a first polarity
with respect to the common voltage and the second pixel voltage has a second polarity with
respect to the common electrode different from the first polarity.

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cont.
26. (New) The method of claim 25, wherein the step of controlling the first data
signal and the second data signal comprises the step of providing the first data signal of the first
polarity and the second data signal of the second polarity to simultaneously increase the first
difference and the second difference.

27. (New) The method of claim 25, wherein the step of controlling the first data
signal and the second data signal comprises the step of providing the first data signal of the
second polarity and the second data signal of the first polarity to simultaneously decrease the
first difference and the second difference.

28. (New) The method of claim 24, wherein the first pixel voltage has a first polarity
with respect to the common voltage and the second pixel voltage has the first polarity with
respect to the common voltage.

29. (New) The method of claim 28, wherein the step of controlling the first data signal and the second data signal comprises the step of providing the first data signal of the first polarity and the second data signal of the first polarity to simultaneously increase the first difference and the second difference.

30. (New) The method of claim 28, wherein the step of controlling the first data signal and the second data signal comprises the step of providing the first data signal of a second polarity and the second data signal of the second polarity to decrease the first difference and the second difference.

31. (New) The method of claim 24, wherein the first pixel electrode and the second electrode are adjoining each other.

32. (New) The method of claim 24, wherein the LCD has more than two gate line blocks.

33. (New) A liquid crystal display (LCD), comprising:
a first gate line block including a first pixel electrode storing a first pixel voltage;
a second gate line block including a second pixel electrode and storing a second pixel voltage;
a common electrode transmitting a common voltage;

a first data line formed in the first gate line block and transmitting a first data signal, said first data signal influencing a first difference between the common voltage and the first pixel voltage stored in the first pixel electrode;

a second data line formed in the second gate line block and transmitting a second data signal, said second data signal influencing a second difference between the common voltage and the second pixel voltage; and

a data driver controlling the first data signal and the second data signal to simultaneously increase or decrease the first difference and the second difference.

34. (New) The LCD of claim 33, wherein the first pixel voltage has a first polarity with respect to the common voltage and the second pixel voltage has a second voltage with respect to the common voltage different from the first polarity.

35. (New) The LCD of claim 34, wherein the data driver provides the first data signal of the first polarity and the second data signal of the second polarity to simultaneously increase the first difference and the second difference.

36. (New) The LCD of claim 34, wherein the data driver provides the first data signal of the second polarity and the second data signal of the first polarity to simultaneously decrease the first difference and the second difference.

37. (New) The LCD of claim 33, wherein the first pixel voltage has a first polarity with respect to the common voltage and the second pixel voltage has the first polarity with respect to the common voltage.

38. (New) The LCD of claim 37, wherein the data driver provides the first data signal of the first polarity and the second data voltage of the first polarity to simultaneously increase the first difference and the second difference.

39. (New) The LCD of claim 37, wherein the data driver provides the first data signal of the second polarity and the second data voltage of the second polarity to simultaneously decrease the first difference and the second difference.

40. (New) The LCD of claim 33, wherein the first pixel electrode and the second pixel electrode are adjoining each other.

41. (New) The LCD of claim 33, wherein the data driver comprising:
a first data driver connected to the first data line for transferring the first data line thereto;
and
a second data driver connected to the second data line for transferring the second data line thereto.

42. (New) The LCD of claim 33, wherein the LCD has more than two gate line blocks.

43. (New) A liquid crystal display (LCD), comprising:

a first gate line block comprising:

a plurality of first gate lines;

a first pixel electrode storing a first pixel voltage; and

a first data line transmitting a first data signal, the first data signal influencing a first difference between the common voltage and the first pixel voltage stored in the first pixel electrode;

a second gate line block comprising:

a plurality of second gate lines;

a second pixel electrode storing a second pixel voltage; and

a second data line separated from the first data line and transmitting a second data signal, the second data signal influencing a second difference between the common voltage and the second pixel voltage stored in the second pixel electrode;

a data driver controlling the first data signal and the second data signal to simultaneously increase or decrease the first difference and the second difference; and

a gate driver connected to the plurality of first gate lines and the plurality of second gate lines and scanning the plurality of first gate lines in a first direction and the plurality of second gate lines in a second direction different from the first direction.

Cancel.